REMARKS

The office action of January 28, 1999 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-20 remain pending. Claims 10-12 and 15-20 have been withdrawn from consideration, but may be reconsidered upon allowance of a generic claim under 37 CFR § 1.141.

Applicant has amended the specification to correct minor informalities discovered therein. The claims have been amended to correct minor informalities therein and to otherwise better clarify the invention. Also, applicant is submitting herewith a Request For Approval of Drawing Changes to correct two informalities discovered in the drawings. Approval of these changes is respectfully requested.

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,471,373 to Shimizu et al. (Shimizu). Claims 3-9 and 13-14 were rejected under 35 U.S.C. § 103(a) as being obvious over Shimizu. Applicant respectfully traverses this rejection.

The action alleges that Shimizu discloses all the features of a semiconductor integrated circuit device recited in claims 1 and 2 relying on Shimizu Figures 1-3 and 18 and a semiconductor substrate (10), transistors Q1, Q2, QE1, QE2, QE3, including gate insulation films of different thicknesses, a terminal for external connection 5 formed on the substrate, and a transistor QE2 allegedly directly connected to the terminal 5 and being a transistor other than the transistor having the thinnest gate insulation film.

Claim 1 includes, among other features, a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed and an

input/output terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal is one of the transistors than a transistor having the thinnest gate insulation film. Several advantages can be realized by the claim 1 combination of features. For example, transistors having gate oxide films of two or more different thicknesses can be integrated within one chip without any deterioration in the transistor characteristics, and the breakdown voltage against ESD (electro-static discharge) can be remarkably enhanced.

Shimizu discloses a technique in which a MIS type transistor having a thin gate oxide film is used in a low voltage circuit portion for performing the reading operation and a MIS type transistor having a thick gate oxide film is used in a high voltage circuit portion for performing the writing operation in an EPROM, thereby implementing high speed reading. Shimizu however, discloses nothing about the advantages of the present invention or about structural features to realize the advantages of the present invention described above.

The action contends that the transistor QE2 (in FIG. 18 of Shimizu) which is to be connected to terminal 5 (in FIG. 1 of Shimizu) shows a transistor connected "directly" to the input/output terminal as recited in the claim 1 invention. According to FIG. 18 and the corresponding description at column 6, line 66 to column 7, line 10 of Shimizu, the transistor QE2 is used for the writing operation, and is connected with an interconnection layer 31. There is no teaching or suggestion that the transistor QE2 is *connected directly* to terminal 5 (in FIG. 1). Similarly, Shimizu is totally silent as to the transistor QE3 being *connected directly* to the power supply terminal as called for in claim 2. For at least these reasons, Shimizu lacks a teaching of all the features recited in claims 1 and 2.

To show claim 3, the action alleges that it would have been obvious to one skilled to couple a power supply line to a respective ground line. Even assuming, but not admitting, that a power supply line can be coupled to a respective ground line, Shimizu fails to disclose a transistor *connected directly* to the input/output terminal, the transistor being one of the transistors other than a transistor having the thinnest gate insulation film as called for in claim 3.

Regarding claims 4-9, 13 and 14, the action contends it would have been obvious to one skilled in the art to construct an interface between circuits for the purpose of creating a buffer between the low and high voltage regions of the circuit. Even assuming, but not admitting, that it would have been obvious to construct the interface between circuits for the purpose of creating a buffer between the low and high voltage regions of the circuit, Shimizu lacks a teaching of a transistor connected directly to an input/output terminal, the transistor being one of the transistors other than a transistor having the thinnest gate insulation film.

CONCLUSION

All rejections having been addressed, applicant respectfully submits that the instant application is in condition for allowance, and solicits prompt notification of the same.

Respectfully submitted,

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Date: April 26, 1999

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